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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,221	06/30/2003	Oh-Sung Song	SEC.559RE	1783
20987	7590	09/19/2005		
VOLENTINE FRANCOS, & WHITT PLLC ONE FREEDOM SQUARE 11951 FREEDOM DRIVE SUITE 1260 RESTON, VA 20190			EXAMINER FOURSON III, GEORGE R	
			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Period for Reply

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-8 is/are allowed.
- 6) ☒ Claim(s) 9-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 6/3/03
 4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____
 5) ☐ Notice of Informal Patent Application (PTO-152)
 6) ☐ Other: _____

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9,10,12,13,14,15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fulford, Jr. et al, Sheng et al and Tsai et al.

Fulford, Jr. et al discloses forming polysilicon gate 12 over gate insulating layer 20 on semiconductor substrate 22, injecting low concentration of impurity ions 21 to form LDD regions 23, forming oxide buffer layer 24 over the substrate, forming sidewall spacers 28 on a portion of the buffer layer, injecting a high concentration of impurity ions 32 to form heavily doped regions 34 having the same conductivity type as regions 23 wherein regions 23 and 34 form source/drain structures, removing an exposed portion of buffer layer to expose the substrate and performing a salicide process which, by definition, involves deposition of a metal layer and subsequent heating to form a silicide by reaction of the metal layer and the portions of the substrate and gate contacting the metal layer (figures 1-6 and col.8, lines 45-55). The buffer layer is disclosed to prevent contamination (col.6, line 31).

The reference does not clearly disclose the conductivity type of the substrate, the formation of the buffer layer by deposition or the identity of the metal layer being a transition metal layer.

In a similar process wherein an exposed portion of buffer layer 50 is removed to perform a salicide process Tsai et al discloses the substrate being of opposite conductivity type to that of the source/drain regions and use of Ti, Co or Ni as the silicide forming metal layer 80 (fig.8).

Sheng et al discloses formation of oxide buffer layer 24 by either of oxidation or by deposition to prevent contamination (col.4, lines 60-68).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fulford, Jr. et al and Tsai et al to enable the disclosed formation of the transistor of Fulford, Jr. et al having the structure of a depletion mode transistor and to enable the disclosed salicide process to be performed according to the teachings of Tsai et al. It would have been obvious to one of ordinary skill in the art to combine the teachings of Fulford, Jr. et al and Sheng et al to enable the disclosed formation of buffer layer 24 of Fulford, Jr. et al to be performed according to the teachings of Sheng et al such that contamination is mitigated.

One of ordinary skill in the art would have been led to the recited thickness of the oxide buffer layer through routine experimentation to provide the desired degree of protection from contamination. Further, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fulford, Jr. et al, Sheng et al and Tsai et al as applied to claims 9,10,12,13,14,15 and 17 above, and further in view of either one of Hadjizadeh-Amini or Chang et al.

None of Fulford, Jr. et al, Sheng et al and Tsai et al disclose the buffer layer being nitride.

Hadjizadeh-Amini discloses use of a nitride buffer layer when forming oxide spacers to achieve the desired etch selectivity necessary to form the spacers (col.4,lines 9-30). Chang et al discloses use of a nitride buffer layer when forming oxide spacers to achieve the desired etch selectivity necessary to form the spacers (col.5, lines 1-10).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Fulford, Jr. et al and either one of Hadjizadeh-Amini or Chang et al to enable the disclosed buffer layer and spacer formation steps of Fulford, Jr. et al to be performed according to the teachings of either one of Hadjizadeh-Amini or Chang et al.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

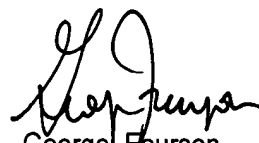
Any inquiry concerning this communication or earlier communications from the examiner should be directed to George Fourson whose telephone number is (571) 272-1860. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from

Art Unit: 2823

either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'George Fourson', written in a cursive style.

George Fourson
Primary Examiner
Art Unit 2823

GFourson
September 14, 2005